SPECIFICATION AMENDMENT

1. Please replace the paragraph [0054] on page 16 with the following amended paragraph:

[0054] Since the pnp-transistor PNP - as can be seen from the layer construction in Fig. **[[2]] 9** - does not form a parasitic diode to the p-substrate, which forms a conductive connection or a short to the reference potential input GND at a polarizing of the output OUT, it does not have to be protected. Therefore, the pJFET, as illustrated in Fig. 1, is preferably only inserted in the path of the npn-transistor NPN between the output OUT and the reference potential input GND and not also in the path between the collector cp of the pnp-transistor PNP and the output OUT.